DYLAN LEIFER-IVES

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OBJECTIVE

Highly driven Computer Engineering Student, focused on compilers and computer architecture. Eager to research into optimization, synthesis, and verification for both programs & compiler-architecture interaction. With experience in AI related optimization both by hardware and compiler.

EDUCATION

Graduate student at California Polytechnic State University: San Luis Obispo (**June 2026)**
Bachelors of Science in Computer Engineering: California Polytechnic State University: San Luis Obispo (**Cum Laude**)

Relevant Coursework: Compiler Design, Computer Architecture, Systems Programming, UXIX, Embedded Systems, FPGA Design, Digital Design, Electronics, Electric Circuit Analysis & Lab I-III

Skills: C \ C++, python, Java, Logic Analyzer, Debugging, Version Control, Git, Microcontrollers, Verilog, VHDL, KiCad, Autodesk Eagle, LtSpice

PROFESSIONAL EXPERIENCE

Fluke Corporation

Employee: June 2024 - September 2024 | Everett, WA, USA

- Coordinated with cross functional teams to design and implement CI/CD automated firmware testing architecture and framework
- Worked on Code Synthesis & Validation to translate in house testing programming language to python.
- Created documentation and presentations for stakeholders for VOC to drive consistently integratable work, and workflows
- Worked on a source to source compiler to remove legacy in house language and code system
- Used Agile methodologies to quickly iterate and integrate new development with both legacy and existing systems
- Coordinated teams and developed standard works for hardware testing
- Digital multimeters, calibrators
- EAR compliances, security measures coventry for security from henry, secure product development with the systems of Fluke.
- Collaborated effectively within large teams, ensuring seamless alignment with plans.
- Improved company’s legacy design tools through programming, achieving a daily time-saving of 30 minutes.

Ace Hardware

Employee: June 2023 - September 2023 | Fairfax, CA, USA

Customer support and sales. Also managed and worked in inventory, receiving, and IT.

Glumac

Electrical Engineering Intern: June 2022 - September 2022 | San Francisco, CA, USA

PROJECTS

Minilang Compiler | Zig, C, minilang **March 2024 - June 2024**

Minilang is a toy language used at Cal Poly for teaching compiler design, it is C like.

- An optimizing compiler written completely from scratch in Zig. Supports armV8 and LLVM as backends.
- Written as a group of two using Agile & Test Driven Development methodologies. With SSA and stack transformations.
- Developed custom IR to support easy & modular implementation of backends. With per backend verification steps.

Arduino ML accelerator | SystemVerilog, IC design, FPGA **February 2023 - June 2023**

A test project to work on application of Computer Architecure to AI.

- Developed using Xilinx tools, embedded FGPA ML accelerator for an Arduino Mega over SPI.
- Reduced running time for letter classification 30% when compared with MCU only solution

RiskBoy | SystemVerilog, Verilog, RISC-V **September 2022 - January 2023**

A project to implement a full RISC-V cpu and custom GPU to run games.

- Handheld gaming console, written from scratch in System Verilog to run on the Artix 7 FPGA, supporting RISC-V ISA
- Custom 5 stage instruction pipeline, and 3 stage graphics pipeline to efficiently run graphical programs with a focus on games.

Dynamic Accelerator | FPGA, LLVM, Spatial Architecture & AI/ML **August 2024 - June 2025**

A project to dynamically compile FPGA accelerators to work in tandem with embedded chip (Arm/RISC-V)

- Spatial architecture implementation interwoven with a RISC-V base, allowing dynamic hardware acceleration.
- Using LLVM to detect highly optimizable code regions and translating them to HSL to run very efficiently on custom spatial computing architecture.

8086 Laptop | C, x86ASM, UNIX **September 2023 - Present**

A Laptop based around the 8086 chip from the 70's

- Designed and fabricated custom PCB board layout and design.
- Custom event based OS written in C. Utilizing TDD to do shift left testing.

Interests: Computer Architecture, Embedded Systems, Verilog, C, C++, Figure Drawing, Olympic Lifting, Hacking old technology, Linguistics, Systems Programming